ETL lpGBT Initial Communication w/Serenity

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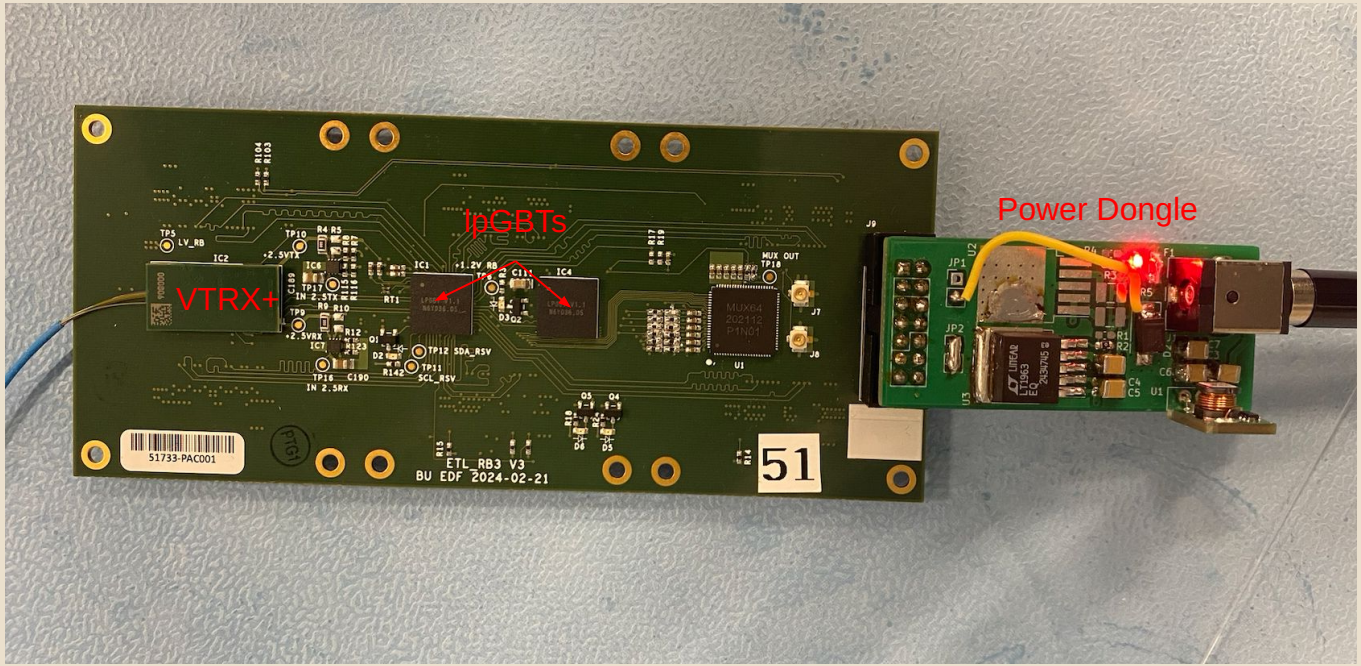
ETL - Readout Board



Master lpGBT v1 Settings

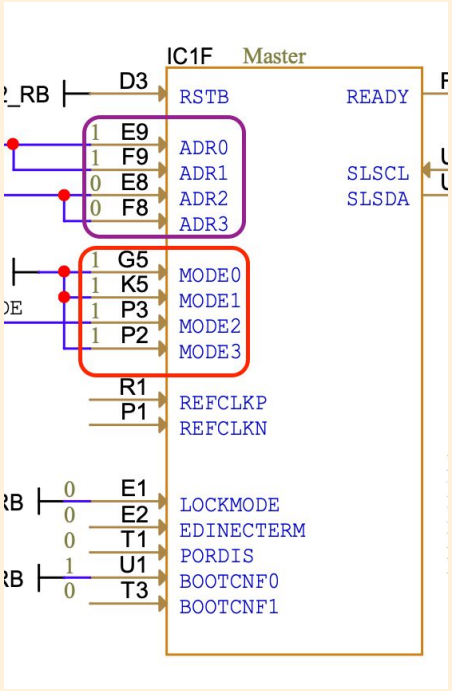


Table 3.1 MODE pins decoding.

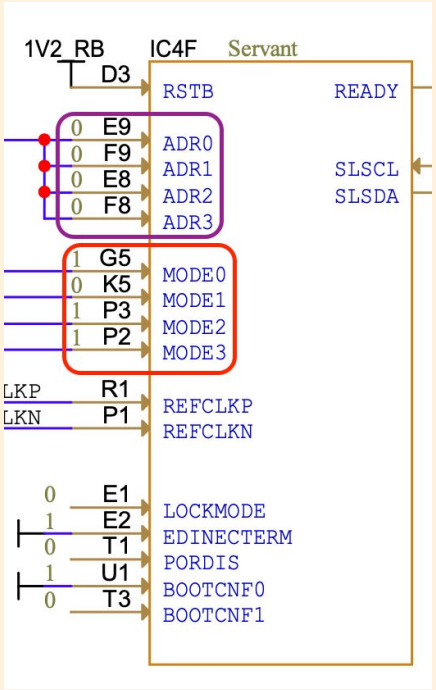
MODE [3:0]	Tx Data Rate	Tx Encoding	lpGBT Mode
4'b0000	5 Gbps	FEC5	Off
4'b0001	5 Gbps	FEC5	Simplex TX
4'b0010	5 Gbps	FEC5	Simplex RX
4'b0011	5 Gbps	FEC5	Transceiver
4'b0100	5 Gbps	FEC12	Off
4'b0101	5 Gbps	FEC12	Simplex TX
4'b0110	5 Gbps	FEC12	Simplex RX
4'b0111	5 Gbps	FEC12	Transceiver
4'b1000	10 Gbps	FEC5	Off
4'b1001	10 Gbps	FEC5	Simplex TX
4'b1010	10 Gbps	FEC5	Simplex RX
4'b1011	10 Gbps	FEC5	Transceiver
4'b1100	10 Gbps	FEC12	Off
4'b1101	10 Gbps	FEC12	Simplex TX
4'b1110	10 Gbps	FEC12	Simplex RX
4'b1111	10 Gbps	FEC12	Transceiver

Table 3.2 lpGBT I2C/IC/EC address

ChipAddressBar[2:0]	ADR3	ADR2	ADR1	ADR0	Chip address[6:0]
3'b000	**1'b0**	**1'b0**	**1'b0**	**1'b0**	**7'b1110000**
3'b000	1'b0	1'b0	1'b0	1'b1	7'b1110001
3'b000	1'b0	1'b0	1'b1	1'b0	7'b1110010
3'b000	1'b0	1'b0	1'b1	1'b1	7'b1110011
3'b000	1'b0	1'b1	1'b0	1'b0	7'b1110100
3'b000	1'b0	1'b1	1'b0	1'b1	7'b1110101
3'b000	1'b0	1'b1	1'b1	1'b0	7'b1110110
3'b000	1'b0	1'b1	1'b1	1'b1	7'b1110111
3'b000	1'b1	1'b0	1'b0	1'b0	7'b1111000
3'b000	1'b1	1'b0	1'b0	1'b1	7'b1111001
3'b000	1'b1	1'b0	1'b1	1'b0	7'b1111010

Uplink (lpGBT Tx): 10.24 Gbps, FEC12 **Downlink (lpGBT Rx):** 2.56 Gbps, Address: 7'b1110011 = 0x73

Servant lpGBT v1 Settings



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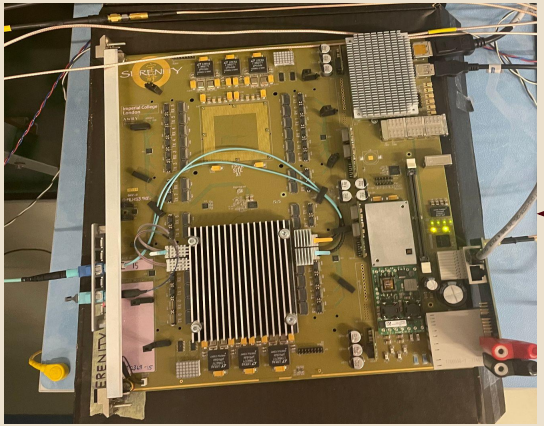
3'b000	1'b0	1'b0	1'b0	1'b1	7'b1110001
3'b000	1'b0	1'b0	1'b1	1'b0	7'b1110010
3'b000	1'b0	1'b0	1'b1	1'b1	7'b1110011
3'b000	1'b0	1'b1	1'b0	1'b0	7'b1110100
3'b000	1'b0	1'b1	1'b0	1'b1	7'b1110101
3'b000	1'b0	1'b1	1'b1	1'b0	7'b1110110
3'b000	1'b0	1'b1	1'b1	1'b1	7'b1110111
3'b000	1'b1	1'b0	1'b0	1'b0	7'b1111000
3'b000	1'b1	1'b0	1'b0	1'b1	7'b1111001
3'b000	1'b1	1'b0	1'b1	1'b0	7'b1111010
3'b000	1'b1	1'b0	1'b1	1'b1	7'b1111011
3'b000	1'b1	1'b1	1'b0	1'b0	7'b1111100
3'b000	1'b1	1'b1	1'b0	1'b1	7'b1111101
3'b000	1'b1	1'b1	1'b1	1'b0	7'b1111110
3'b000	1'b1	1'b1	1'b1	1'b1	7'b1111111
...	...	...	...	...	...
3'b001	1'b0	1'b0	1'b0	1'b0	7'b1100000

Uplink (lpGBT Tx): 10.24 Gbps, FEC12 **Downlink (lpGBT Rx):** 2.56 Gbps, Address: 7'b1100000 = 0x60

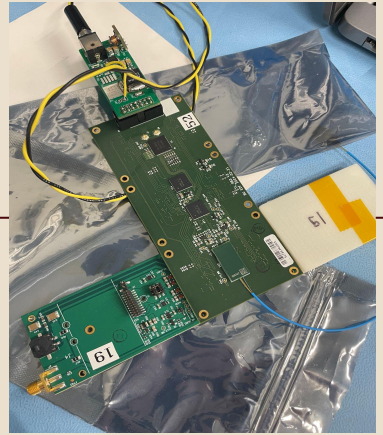
Setup



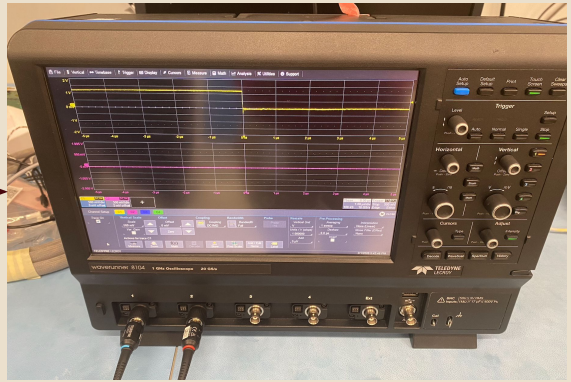
Serenity Z1.1

Firmware: lpGBTv2_3_SO1_ceacmsfw_250603_1554_ETL (FEC12)

RBv3



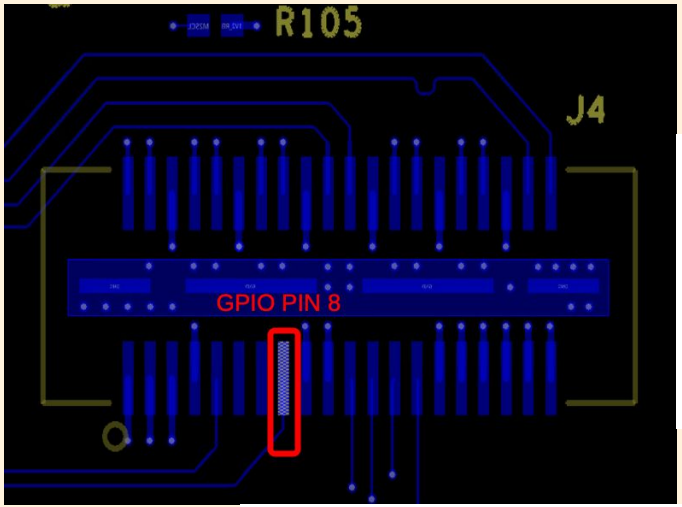
Oscilloscope



Goal 1: Control a GPIO Pin on Master lpGBT

Why?

- No configuration required at all (Tested with KCU105 + Tamalero)
- Test lpGBT Rx
  - IC address
  - Link number
  - Is the downlink information being correctly sent/received
- 3 blind writes



[0x055] PIOOutH

Output control for Parallel IO port (when pin is configured as output).

- **Bit 7:0 - PIOOut[15:8] -**

PIOOut[n]	Output
1'b0	Low
1'b1	High

[0x053] PIODirH

Direction control for Parallel IO port.

- **Bit 7:0 - PIODir[15:8] -**

PIODir[n]	Function
1'b0	Pin configured as an input
1'b1	Pin configured as an output

Outcomes: GPIO Tests

- To accomplish a blind write we need to wrap the functions in try/catch blocks because the C++ functions try to read after every write which results in a timeout error
- Master address : 0x73; Link: 4
- Downlink seems to correctly propagate data from Serenity and lpGBT can understand the incoming downlink data

Goal 2: Run MTD SW with Correct Settings

```
{
  "Master LPGBT": {
    "connection": "/home/cmx/mtd-emp-toolbox/mtd-daq/lpGBTv2_3_SO1_ceacmsfw_250225_0031/hls_connections.xml",
    "link": 0,
    "address": "0x60",
    "fpga": "x0",
    "configurations": {
      "EPRX": {
        "nelinksxegroup": 4,
        "neprxegroups": 7,
```

Why?

- Database had incorrect values for address, link, and connections file for ETL
- See if running lpgbt_main.py can correctly lock onto master lpgbt with correct values

Outcomes: MTD

- After inverting polarity of the link and forcing blind writes for all config registers the first read results in a timeout error
- Failed at: Config_done_and_wait_for_ready()
  - PUSMStatus
- Uplink data is not being received or is not being decoded correctly, cannot lock onto lpGBT
- Full info: Test Report

```
  File "/home/cmx/DAQ/lpgbt_control_lib/lpgbt_control_lib/lpgbt.py", line 145, in w
    self.write_regs(reg_addr, [reg_val])
  File "/home/cmx/DAQ/lpgbt_control_lib/lpgbt_control_lib/lpgbt.py", line 80, in de
    raise error
  File "/home/cmx/DAQ/lpgbt_control_lib/lpgbt_control_lib/lpgbt.py", line 77, in de
    retval = method(self, *args, **kwargs)
             ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
  File "/home/cmx/DAQ/lpgbt_control_lib/lpgbt_control_lib/lpgbt.py", line 157, in w
    self._comm_intfs[comm_intf]["write_regs"](reg_addr=reg_addr, reg_vals=reg_vals)
  File "/home/cmx/etl/toolbox/mtd-emp-toolbox/fresh-mtd-daq/src/mtddaqsw/controller
    self.lpgbt_com.ic_write(
  File "/home/cmx/etl/toolbox/mtd-emp-toolbox/fresh-mtd-daq/src/mtddaqsw/controller
    self.SCCIC.icWriteBlock(addr, values, lpgbt_addr)
emp._emp_python.exception: SCCICNode: Timed out waiting for replies (expecting 1 wo
```

Conclusions / Next Steps

- Downlink is working (can send data and lpGBT understands and correctly reacts to incoming data); Uplink is not working as Serenity does not receive and data or does not understand the data coming from the uplink
- Configuration of lpGBT on working ETL firmware (KCU105) + Tamalero software is different then how Serenity + MTD software configures the lpGBT before performing first register read: old presentation
    - **Next Test**: Configure the lpGBT the same way Tamalero does using Serenity + MTD software while forcing blind writes. Then try to read the ROMREG
- Check uplink data path in firmware in more detail, how does ETL KCU105 firmware decode and prepare lpGBT incoming data vs Serenity (Is FEC12 being decoded correctly?)

Questions
Comments
Suggestions