ETL IN MTD DAQ UPDATE

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MUX64 FULLY OPERATIONAL ON MTD SW

```
[cmx@serenity-2368-15 mux64]$ python -m src.mtddaqsw.apps.S_mux64
Fetching config from: http://localhost:8001/etl_chip_config/Master LPGBT
Success: Received configuration for Master LPGBT
Fetching config from: http://localhost:8001/etl_chip_config/MUX64
Success: Received configuration for MUX64
Calibrated lpgbt  ADC. Gain: 1.87109375 / Offset: 502
```

Channel	Pin	Voltage	Comment
LV_RB	0	8.97089	Low voltage, 9V
RT2	1	1.07346	lpGBT ADC5 (RT2), R2 values is approximate
slot0_a4	2	0.0335031	VREF3 on module 1
slot0_a5	3	0.0335031	VREF2 on module 1
slot0_a6	4	0.0344917	VREF4 on module 1
slot0_a7	5	0.0344917	VREF1 on module 1
slot1_a4	6	0.0335031	VREF3 on module 2
slot1_a5	7	0.0335031	VREF2 on module 2
slot1_a6	8	0.0344917	VREF4 on module 2
slot1_a7	9	0.0335031	VREF1 on module 2
slot2_a4	10	0.0335031	VREF3 on module 3
slot2_a5	11	0.0335031	VREF2 on module 3
slot2_a6	12	0.0335031	VREF4 on module 3
slot2_a7	13	0.0335031	VREF1 on module 3

No Module connected, **Regular**

- Debugged ADC Conversion
- Calibrated LPGBT ADCs
- Verbose Output Option
- Pretty table print
- Proper error handling by using custom error exceptions
- MUX channels read by custom name or one of the 64 physical pin numbers
- Verified ETROC Monitoring - modulev0Bv

```
[cmx@serenity-2368-15 mux64]$ python -m src.mtddaqsw.apps.S_mux64
Fetching config from: http://localhost:8001/etl_chip_config/Master LPGBT
Success: Received configuration for Master LPGBT
Fetching config from: http://localhost:8001/etl_chip_config/MUX64
Success: Received configuration for MUX64
Calibrated lpgbt  ADC. Gain: 1.8671875 / Offset: 502
```

Channel	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Comment
LV_RB	0	814	831.562	0.812867	8.94153	Low voltage, 9V
RT2	1	533	547.952	0.535632	1.07126	lpGBT ADC5 (RT2), R2 values is approximate
slot0_a4	2	24	34.223	0.0334535	0.0334535	VREF3 on module 1
slot0_a5	3	24	34.223	0.0334535	0.0334535	VREF2 on module 1
slot0_a6	4	25	35.2323	0.0344401	0.0344401	VREF4 on module 1
slot0_a7	5	25	35.2323	0.0344401	0.0344401	VREF1 on module 1
slot1_a4	6	24	34.223	0.0334535	0.0334535	VREF3 on module 2
slot1_a5	7	24	34.223	0.0334535	0.0334535	VREF2 on module 2
slot1_a6	8	23	33.2137	0.0324669	0.0324669	VREF4 on module 2
slot1_a7	9	24	34.223	0.0334535	0.0334535	VREF1 on module 2
slot2_a4	10	25	35.2323	0.0344401	0.0344401	VREF3 on module 3
slot2_a5	11	24	34.223	0.0334535	0.0334535	VREF2 on module 3
slot2_a6	12	25	35.2323	0.0344401	0.0344401	VREF4 on module 3
slot2_a7	13	24	34.223	0.0334535	0.0334535	VREF1 on module 3

No Module connected, **Verbose**

MUX64 FULLY WORKING ON MTD SW

```
[cmx@serenity-2368-15 mux64]$ python -m src.mtddaqsw.apps.S_mux64
Fetching config from: http://localhost:8001/etl_chip_config/Master LPGBT
Success: Received configuration for Master LPGBT
Fetching config from: http://localhost:8001/etl_chip_config/MUX64
Success: Received configuration for MUX64
Calibrated lpgbt  ADC. Gain: 1.86328125 / Offset: 502
```

Channel	Pin	Voltage	Comment
LV_RB	0	8.8689	Low voltage, 9V
RT2	1	1.06906	lpGBT ADC5 (RT2), R2 values is approximate
slot0_a4	2	0.033404	VREF3 on module 1
slot0_a5	3	0.989387	VREF2 on module 1
slot0_a6	4	0.458723	VREF4 on module 1
slot0_a7	5	0.0343885	VREF1 on module 1
slot1_a4	6	0.033404	VREF3 on module 2
slot1_a5	7	0.033404	VREF2 on module 2
slot1_a6	8	0.033404	VREF4 on module 2
slot1_a7	9	0.033404	VREF1 on module 2
slot2_a4	10	0.0343885	VREF3 on module 3
slot2_a5	11	0.033404	VREF2 on module 3
slot2_a6	12	0.033404	VREF4 on module 3
slot2_a7	13	0.0343885	VREF1 on module 3

Slot 1 Module, MTD SW

MODULE OUTPUTS WITH A A MODULEV0B **CONNECTED**!

```
RB configured successfully. Rhett is happy
>>> rb.MUX64.read_channels()
```

Channel	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Comment
A0	0	806	564.419	0.807337	8.86981	LV RB
A1	1	543	559.351	0.546776	1.08959	lpGBT ADC5 (RT2), R2 values is approximate
mod0_a5	3	997	1018.47	0.996565	0.995575	VREF on module 1
mod0_a6	4	569	583.676	0.571544	0.571544	VTEMP on module 1
mod1_a5	7	24	32.3243	0.0306069	0.0315976	VREF on module 2
mod1_a6	8	24	32.3243	0.0315976	0.0315976	VTEMP on module 2
mod2_a5	11	25	32.3243	0.0325883	0.0315976	VREF on module 3
mod2_a6	12	25	32.3243	0.0306069	0.0315976	VTEMP on module 3

Slot 1 Module, Tamalero

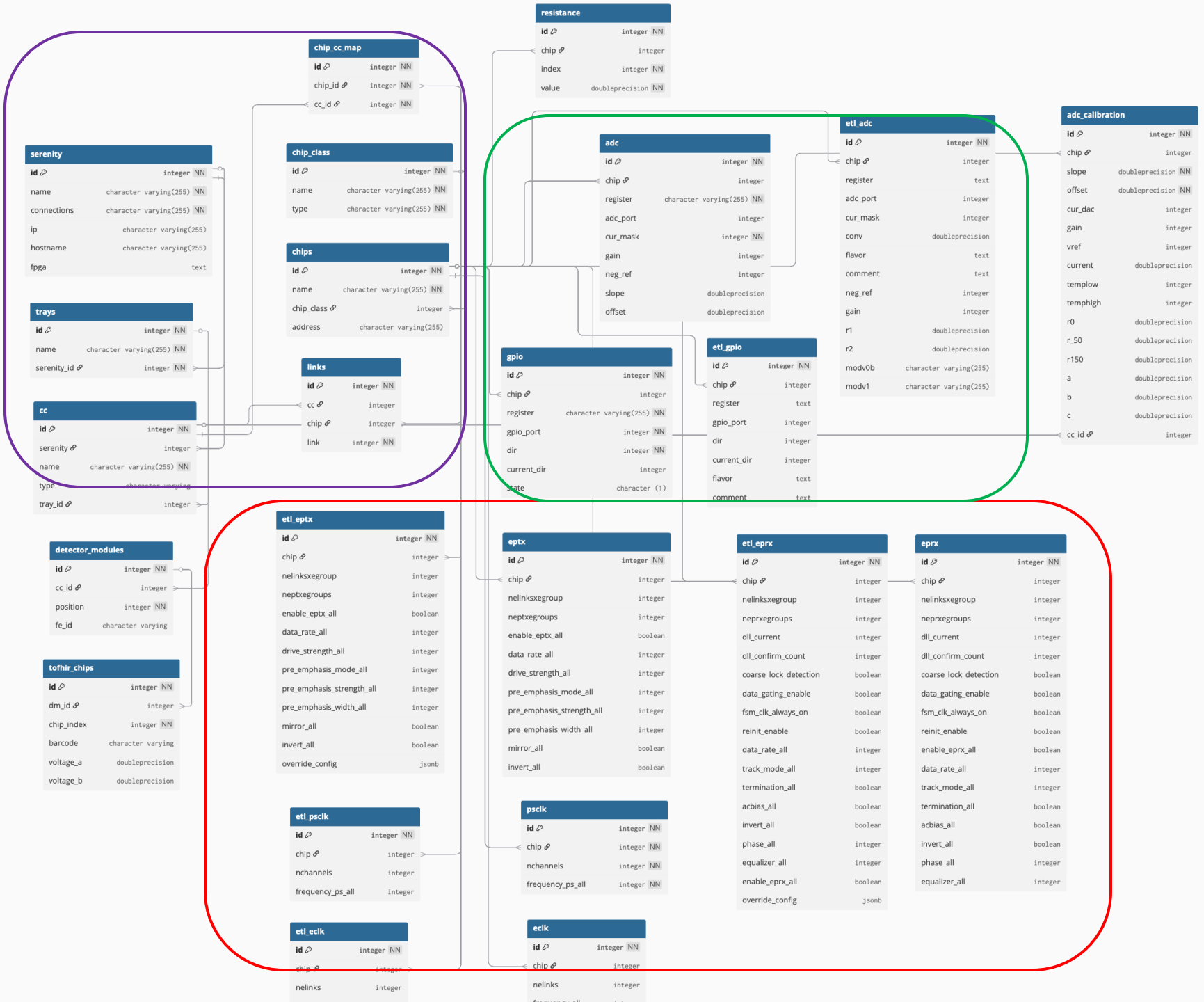
MTD DAQ DATABASE SCHEMA UPDATE FOR LPGBT CONFIGURATION

Problem:

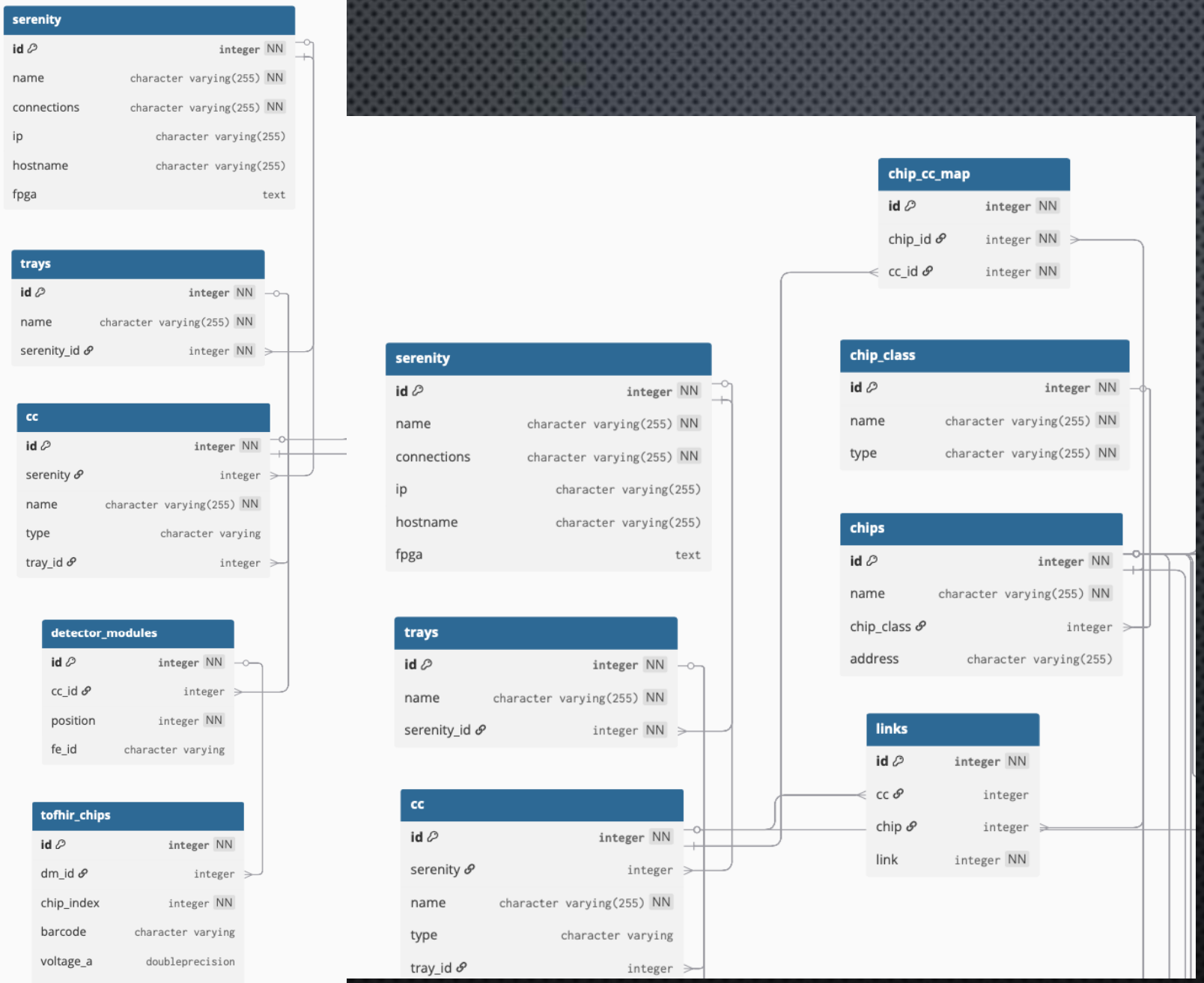
- database schema does not Fully support ETL needs
- For MUX64 we dump LPGBT registers to get it working

Proposal:

- Merge ETL and BTL lpGBT configuration tables into one table
- Store all lpGBT writeable registers in the database



- Goal – {board_name}/{chip_name} gives correct configuration
  - Instead of just the chip name (ex: LPGBT0, MUX64)
- Agree on uniform table schema between ETL and BTL
- Hold all writeable registers lpGBT registers in DB
- Move towards agnostic language, instead of cc table we have board table

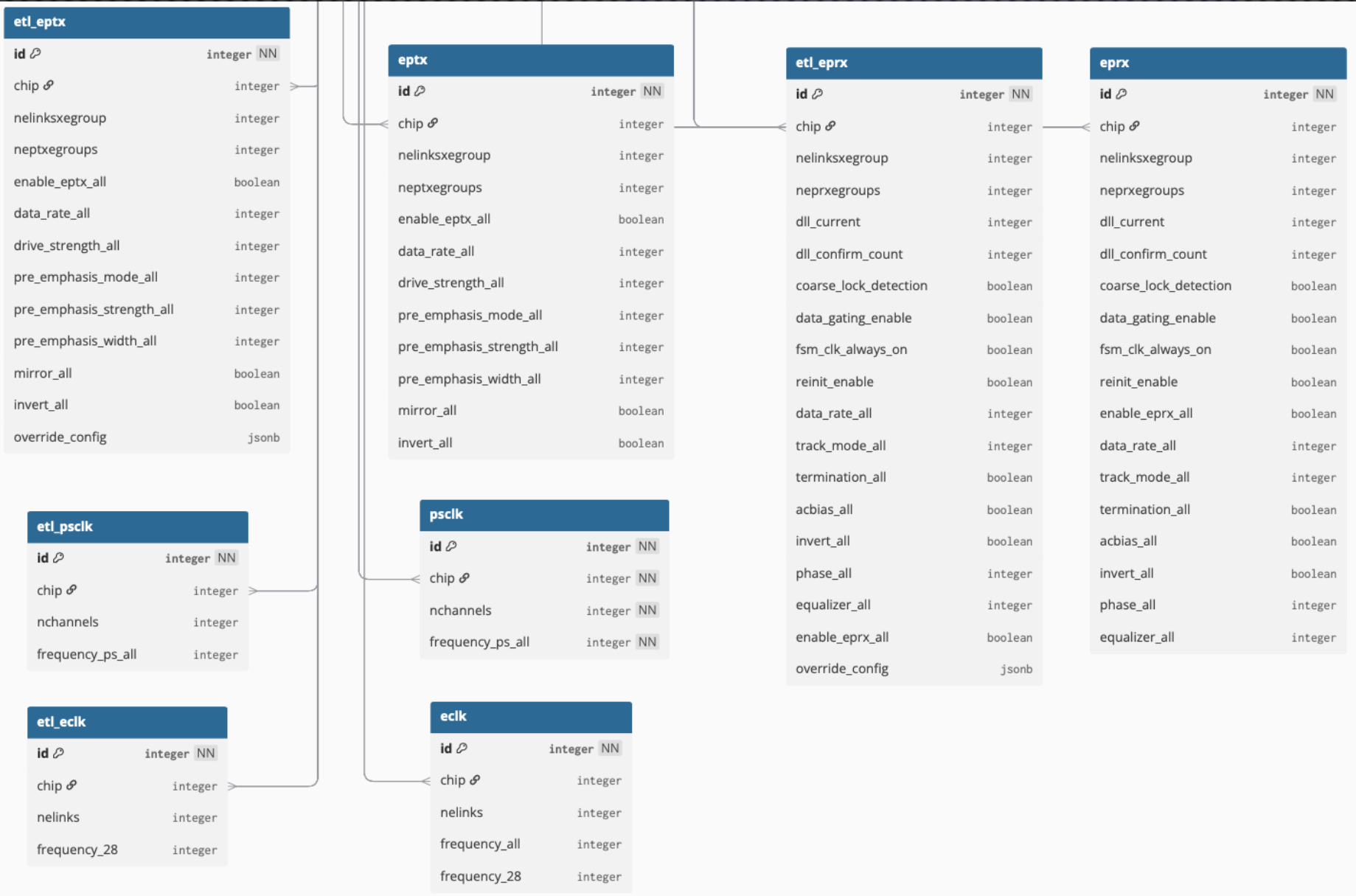


- Goal – {board_name}/{chip_name} gives correct confinguration

Proposing Changes:

- Move towards agnostic language
- Keep relations in order to keep BTL SW and Setup working with minimal Disruptions
- Could possibly use Detecor_module table to point to an ETROC_chips to track connections to RB and Serenity

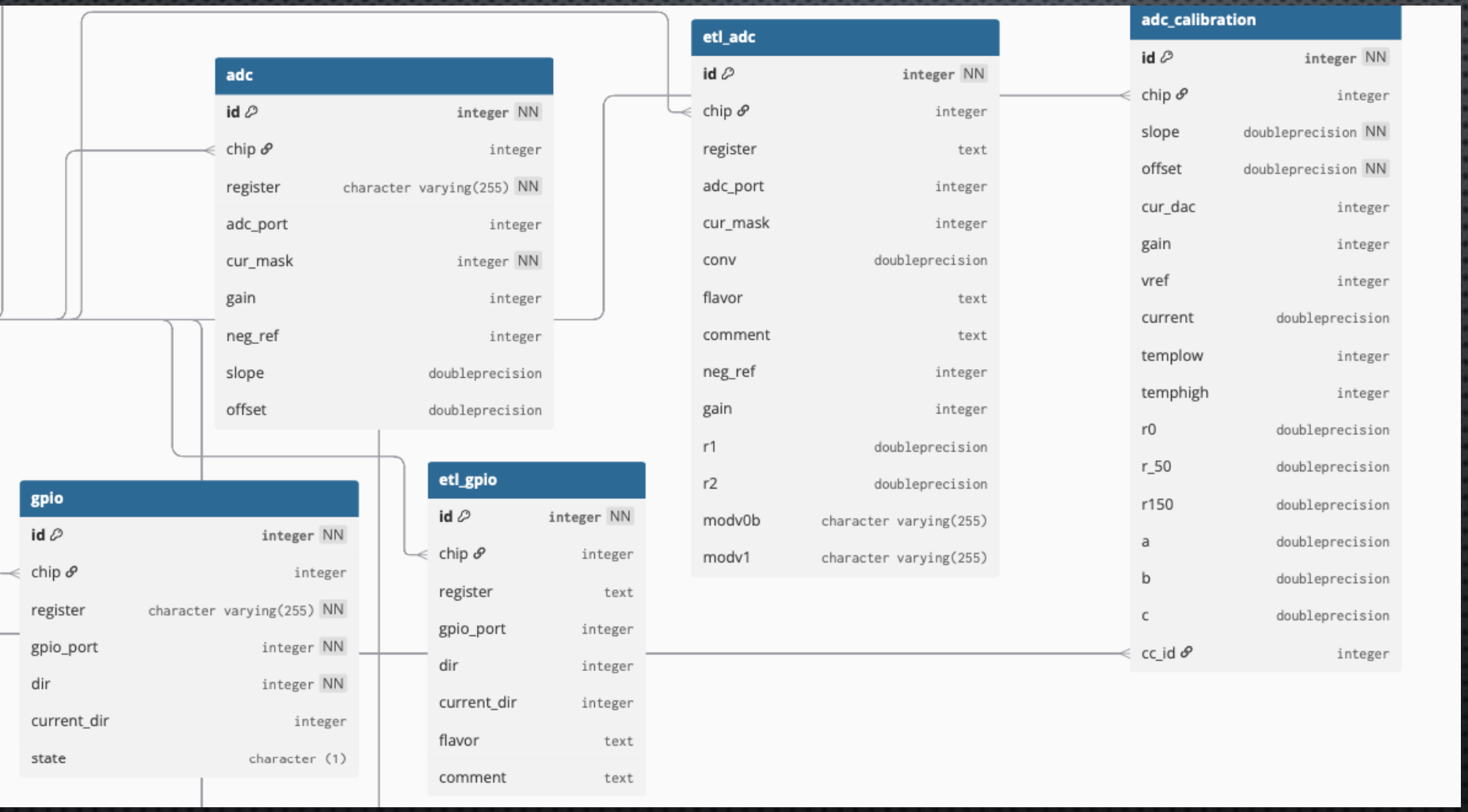
LPGBT REGS CURRENT SCHEMA



PROPOSING CHANGES:

- BOTH ETL AND BTL SHOULD USE SAME SCHEMA
- SINGLE TABLE HOLDS ALL *WRITEABLE REGISTERS*
  - FOLLOW LPGBT DOCUMENTATION FOR CHUNKING THE REGISTERS INTO SEPARATE TABLES
- SW FUNCTIONS ALLOW TO READ/WRITE TO GROUP OR SPECIFIC REGISTERS
  - E.G DATARATE(1) OR DATARATE(1, CH=3)

GPIO/ADC CURRENT SCHEMA



Proposed Changes:

- Both ETL and BTL should use same schema
- ETL_ADC table values should be merged into ADC and ADC Calibration respectively (Based on MTD SW Needs)

TOFHIR TABLES REMAIN UNCHANGED

tofhir_fetp_scan_th_config

id	integer NN
type	text NN
threshold	text NN
pre_window	text NN
post_window	text NN
coincidence_window	text NN
single_fraction	text NN
coincidence_time_window	text NN
group_time_window	text NN
global.c_counter_en	text NN
global.c_counter_t	text NN
channel.c_tgr_main	text NN
channel.c_count	text NN
channel.c_latch_b	text NN
channel.cfg_a2_dcr_delay_e	text NN
channel.c_min_q	text NN
channel.c_max_q	text NN
global.pulse_amplitude	text NN
global.c_ext_tp_en	text NN
global.c_fetp_en	text NN
channel.cfg_a1_fetp_en	text NN

tofhir_disc_scan_config

id	integer NN
type	text NN
threshold	text NN
pre_window	text NN
post_window	text NN
coincidence_window	text NN
single_fraction	text NN
coincidence_time_window	text NN
group_time_window	text NN
global.c_counter_en	text NN
global.c_counter_t	text NN
global.c_l1_enable	text NN
channel.c_tgr_main	text NN
channel.c_count	text NN
channel.c_latch_b	text NN
channel.cfg_a3_range_t1	text NN
channel.cfg_a3_ith_t1	text NN
global.c_aldo_en	text NN
global.c_aldo_range	text NN

tofhir_tp_config

id	integer NN
type	text NN
threshold	text NN
pre_window	text NN
post_window	text NN
coincidence_window	text NN
single_fraction	text NN
coincidence_time_window	text NN
group_time_window	text NN
channel.c_tgr_main	text NN
global.c_tp_en	text NN
global.c_tp_period	text NN
global.c_tp_length	text NN
global.c_tp_inv	text NN

tofhir_ith1_config

id	integer NN
type	text NN
threshold	text NN
pre_window	text NN
post_window	text NN
coincidence_window	text NN
single_fraction	text NN
coincidence_time_window	text NN
group_time_window	text NN
global.c_counter_en	text NN
channel.cfg_a2_dcr_delay_t	text NN
channel.cfg_a2_dcr_delay_e	text NN
channel.cfg_a2_pulse_trim_t	text NN
channel.cfg_a2_pulse_trim_e	text NN
channel.cfg_a2_attenuator_gain	text NN
channel.c_max_v_en	text NN
channel.c_min_q	text NN
channel.c_max_q	text NN
channel.cfg_a3_range_t1	text NN
channel.cfg_a3_range_t2	text NN
channel.c_tgr_t1	text NN
channel.c_tgr_q	text NN
channel.c_tgr_t2	text NN
channel.c_tgr_V	text NN
channel.c_tgr_B	text NN
channel.cfg_a3_ith_t1	text NN
channel.cfg_a3_ith_t2	text NN
channel.cfg_a3_ith_e	text NN
channel.c_tgr_main	text NN
global.c_aldo_en	text NN
global.c_aldo_range	text NN

tofhir_field_metadata

id	integer NN
config_type	text NN
field_name	text NN
section_name	text NN

tofhir_fetp_config

id	integer NN
type	text NN
threshold	text NN
pre_window	text NN
post_window	text NN
coincidence_window	text NN
single_fraction	text NN
coincidence_time_window	text NN
group_time_window	text NN
global.c_counter_en	text NN
channel.c_tgr_main	text NN
global.c_tp_en	text NN
global.c_tp_period	text NN
global.c_tp_length	text NN
global.c_tp_inv	text NN
global.c_fetp_en	text NN
global.pulse_amplitude	text NN
channel.cfg_a1_fetp_en	text NN
channel.cfg_a2_dcr_delay_t	text NN
channel.cfg_a2_dcr_delay_e	text NN
channel.cfg_a2_pulse_trim_t	text NN
channel.cfg_a2_pulse_trim_e	text NN
channel.cfg_a2_attenuator_gain	text NN
channel.c_max_v_en	text NN
channel.c_min_q	text NN
channel.c_max_q	text NN
channel.cfg_a3_range_t1	text NN
channel.cfg_a3_range_t2	text NN
channel.c_tgr_t1	text NN
channel.c_tgr_q	text NN
channel.c_tgr_t2	text NN
channel.c_tgr_V	text NN
channel.c_tgr_B	text NN
channel.cfg_a3_ith_t1	text NN
channel.cfg_a3_ith_t2	text NN
channel.cfg_a3_ith_e	text NN

Next Steps

- I2C Debugging and Working – SERVANT LPGBT and ETROCs
- ETROC Encoder + Decoder in FIRMWARE
- Deploy AND Test New DB Schema on Test Instance DB
  - Add MTD Configurator (API and DB)changes that contains merged routes between ETL and BTL
- Move ADC Calibration to LPGBT Controller