Serenity Link Test

Date: 14 and 15 July 2025
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Background:

Last week we attempted running power-up configuration and controlling LEDs on ETL FE board with Serenity and these tests were successful at controlling LEDs and showed that the **master lpGBT ready light turns on** after writing the power-up configuration.

Due to previous tests supporting the idea that the downlink is correctly sending data (we can control multiple GPIOs, LEDs, and when running power-up the **master lpGBT ready light turns on**) and the fact that whenever we try to read data there is always a timeout error we believe there is an issue on the uplink.

One of these possibilities is we are selecting the wrong link for the uplink (this is due to the fact that the KCU firmware has one downlink and two uplinks, so maybe we are not reading the right uplink on Serenity) **This is what we are testing** in this report

Another possibility is the correct link is being selected but the firmware is incorrectly decoding FEC12 lpgbt data words, theoretically you should still receive some data even though it would be unreadable data.

The final possibility we can think of why the uplink is not working is that the MGT is just not being able to lock correctly and no data is being received or unreadable data is being received but we are not sure of what the expected behavior is when the MGT does not lock.

Tests:

All these tests perform the standard Tamalero initialization (lpGBT power-up configuration) before the first read. Tamalero registers refer to setting registers that are set during MTD power up configuration to the value they are set to by Tamalero instead.

> **Note:** For more detail about
>
> - standard Tamalero initialization: ETL lpGBT Power-up
> - MTD/Tamaleo register differences: MTD vs ETL Power-up
> - MTD init: function

- no MTD init, selecting links `[0,1,2,3,4,5,6,7,8,9,10]`

- with MTD init, selecting links `[0,1,2,3,4,5,6,7,8,9,10]`
- with MTD init, selecting links `[0,1,2,3,4,5,6,7,8,9,10]` + power cycle
- no MTD init, selecting links `[0,1,2,3,4,5,6,7,8,9,10]` + power cycle
- no MTD init, no tamalero registers, links 0 to 24
- no MTD init, no tamalero registers, links 0 to 11
- no MTD init, no tamalero registers, links 0 to 11 + power cycle
- with MTD init, with tamalero registers, links 0 to 11
- with MTD init, with tamalero registers, links 0 to 11 + power cycle
- with MTD init, no tamalero registers, links 0 to 11
- with MTD init, no tamalero registers, links 0 to 11 + power cycle
- with MTD init, no tamalero registers, links 0 to 11, sleep of 0.3 after link switch
- with MTD init, with tamalero registers, links 0 to 11. sleep of 0.1 after link switch
- with MTD init, with tamalero registers, links 0 to 11. sleep of 0.1 after link switch + power cycle
- no MTD init, no tamalero registers, links 0 to 11. sleep of 0.1 after link switch
- no MTD init, no tamalero registers, links 0 to 11. sleep of 0.1 after link switch + power cycle
- with MTD init, no tamalero registers, links 0 to 11. sleep of 0.1 after link switch
- with MTD init, no tamalero registers, links 0 to 11. sleep of 0.1 after link switch + power cycle
- no MTD init, with tamalero registers, links 0 to 11. sleep of 0.1 after link switch
- no MTD init, with tamalero registers, links 0 to 11. sleep of 0.1 after link switch + power cycle

Results:

When running the power up configuration the *lpGBT master ready light* turned on as expected when sending power-up configuration through the downlink. However after writing the power-up configuration on the correct downlink and then cycling through different links to attempt a read still resulted in timeout errors (0 packets recieved). We could only read links 0-11, once we went above 11 the error changed (we assume that this is due to the fact that each link is a tx+rx pair and there is a maximum on 24 lines in one firefly aka maximum of 12 channels).

Next Steps:

Information we need help finding the answer to:

- How does timeout error occur, (when NO data is being received, or NO correctly formatted data)?

- What is the data format that the Serenity expects? Assuming that the datapath packages the data a specific way before sending it to the payload. And assuming that the payload just passes through the data and Serenity just reads the payload, where can we find information of the specific data format Serenity is expecting?
    - My thought process is maybe the data is not being decoded correctly due FEC12 instead of FEC5
- Is there anyone we can talk to, to learn more information on setting up and using the emp butler to help us with debugging other then the documentation online?
- Is there any other debugging tools Serenity or emp framework engineers have already set up other then the emp butler or is there an example of inserting an ILA in the emp framework datapath or payload
    - I have experience inserting ILAs with firmware projects built using HOG but I am not sure how to insert one that ipbb will build and how to see the ILA data from Serenity on a PC

Things we will do in the meantime:

- Review the firmware and see how the uplink data gets decoded in the upper level firmware blocks (Naomi)
- Review the software to understand timeout errors more (Hayden)
- Review emp fw documentation on emp butler for debugging (Naomi)
- Review the physical hardware wired connections we are using for the uplink (does it allow all 12 optical links from the vtrx+?) (Hayden)

What we want to test next:

- Use the emp butler to check link status and connection on serenity firefly
- Can we see the physical raw uplink data bits (with emp butler or ILA) to confirm whether we have garbage data (that is not packaged correctly) vs no data at all in the uplink?
    - If garbage data, lpGBT data might not be decoded or packaged correctly
    - If no data, possible mgt not locking?