

ETL in Serenity with new Setup Test

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Summary

After changing the Serenity fiber connection setup (to now use a cassette and fanout) and cleaning all the fiber wires we can now confirm both the uplink and downlink to the master IpGBT it working. This means we can now read and write to the IpGBT registers.

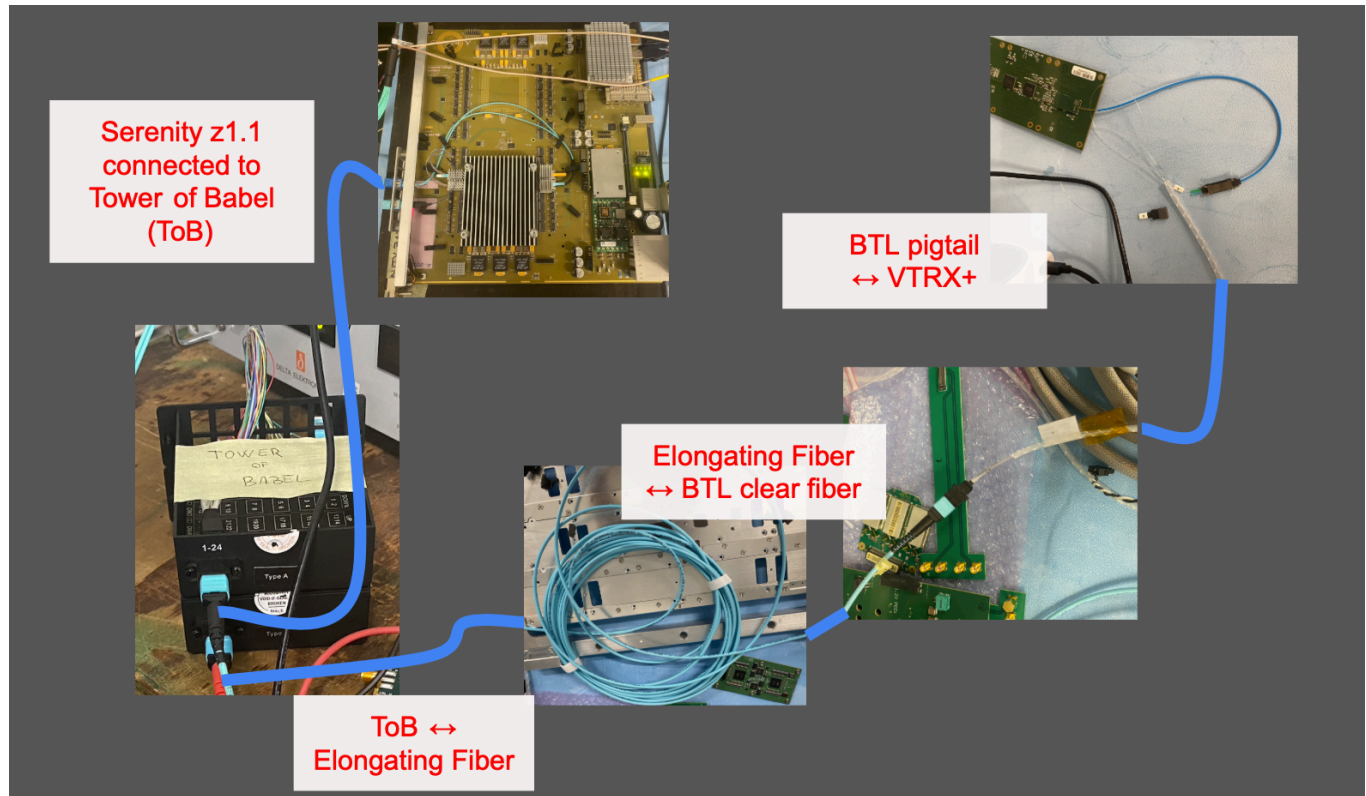
Introduction

After researching more into the physical hardware connections between the Readout Board and Serenity we have realized that one of the BTL fiber wire we are using does not allow for both uplinks from the VTRX+ to be sent to the Tower of Babel which connects to Serenity. After realizing this we wanted to investigate the behavior of the KCU and Tamalero software if only the Master IpGBT uplink is connected to mimic the set-up we have been using with the Serenity. During this test we realized the fibers were extremely dirty so we cleaned all the fibers. After this test proved successful in communicating with the master IpGBT we refactored our optical link setup to avoid using the incompatible BTL fibers and clean all possible fiber connections. This test aims to test the new hardware setup after cleaning the fibers and integrating a cassette with fanout instead of the clear BTL fiber.

Setup

Hardware Fiber Connections

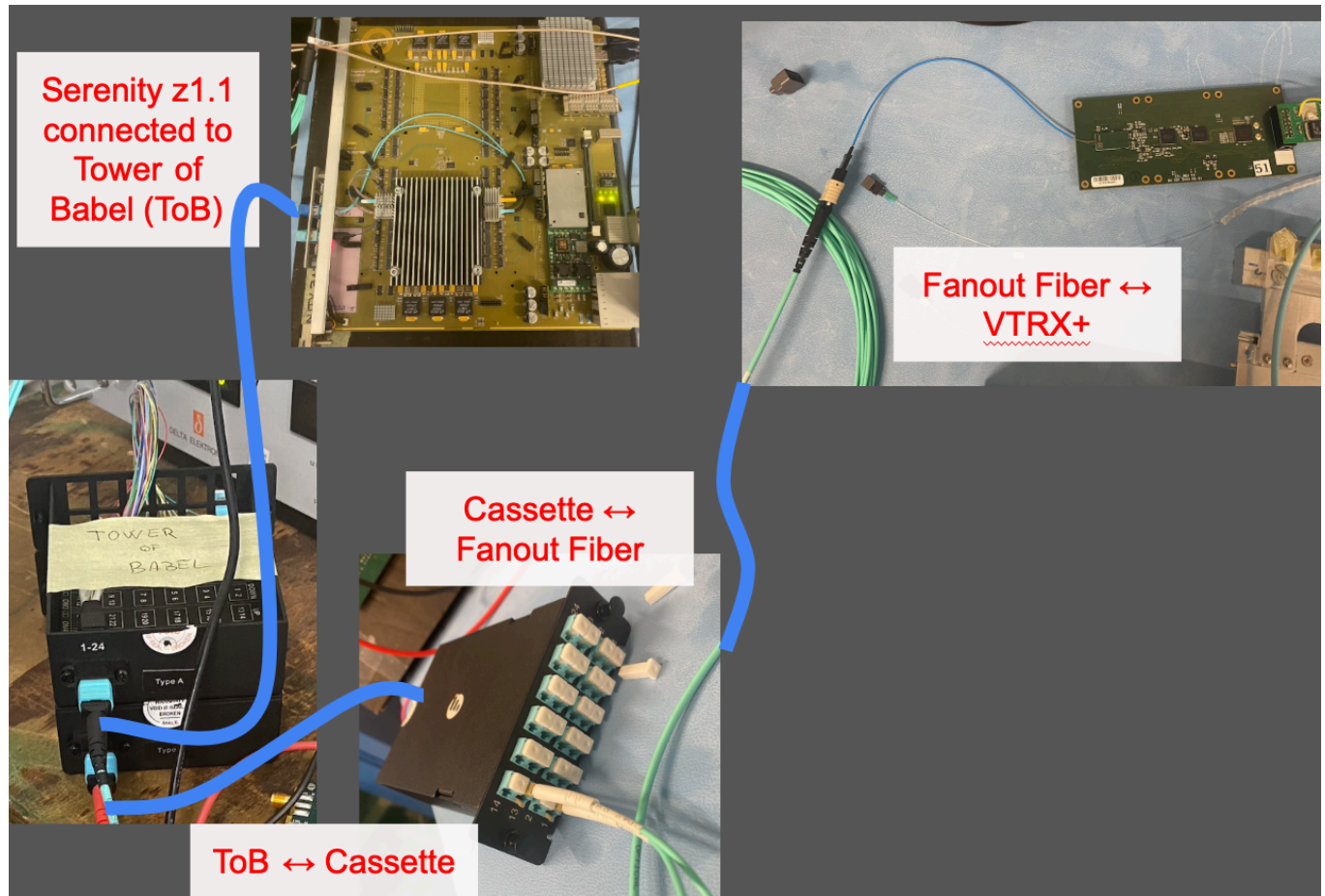
In all previous Serenity test this was our testing set-up which was created by BTL people:



After doing more research on the hardware we realized 2 main problems

1. BTL clear fiber only allows for one uplink per VTRX Connector which is incompatible with our setup since the VTRX tries to send 2 uplinks
2. The elongated fiber was not clean

This is the new setup we used for these tests to address those issues:



Hardware Mapping to Serenity

Here is how the VTRX is connected to the RB based on the schematic:

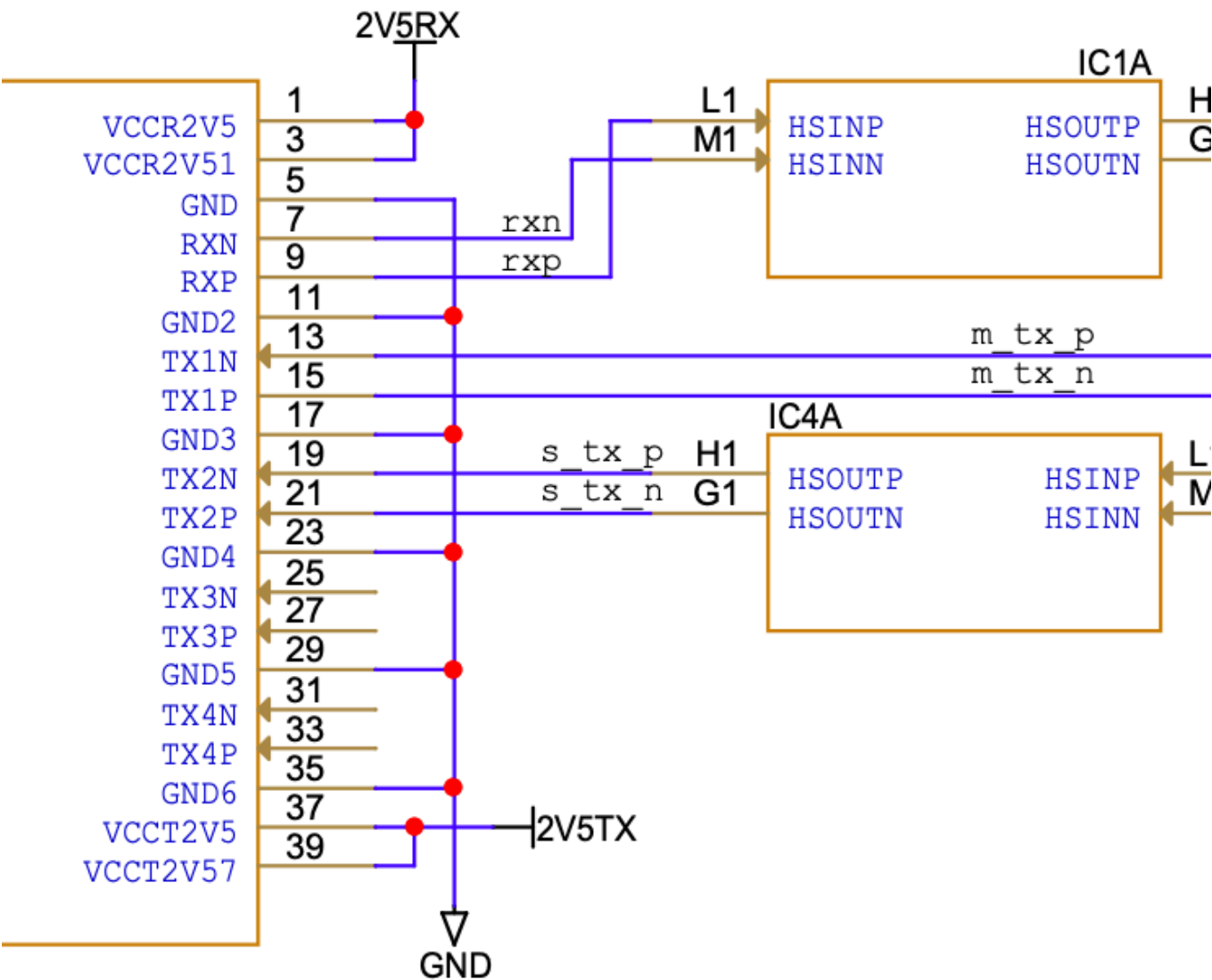


Table 9: VTRx⁺ module optical interface pinout.

VTRx ⁺ Function	Fibre Number
RX	7
TX1	6
TX2	5
TX3	4
TX4	3

Based on the previous 2 images we can concur that to connect only the master IpGBT uplink we would need to plug in fiber number 6 (TX1). And the downlink is fiber number 7.

Procedure

1. Flash Serenity with FEC12 firmware
2. Connect downlink (fiber number 7) to slot 1 in the cassette and then run script that tests toggling LED on RB
 - In the Tower of Babel slot 1 maps to link 4 on the MTD SW so this is what we used to test
 - Can control LED to turn on and off correctly (As seen in previous setup)
 - When writing to IpGBT receive timeout errors (As seen in previous setup)
3. Connect uplink (fiber number 6) to slot 13 and then run script that tests toggling LED on RB
 - Can control LED to turn on and off correctly (As seen in previous setup)
 - NO TIMEOUT ERRORS SEEN (this is new)
4. Power cycled system and tried running the initial configuration script
 - New error was encountered (Never seen in previous setup tests)

```
21-07-25 14:47:57.892493 [140114945260416] WARNING - PCIe client "x0":  
Expected reply packet to contain 3 words, but it actually contains 2 words
```

Note: We had never seen this error before and usually get 0 words the whole time so this was exciting to see

1. Repeat toggling LED with uplink fiber connected to slot 14
 - Can control LED to turn on and off correctly (As seen in previous setup)
 - When writing to IpGBT receive timeout errors (As seen in previous setup)
2. Repeat initial configuration script with uplink fiber connected to slot 14
 - Same new error is seen which is confusing since slot 14 does not map to link 4
3. Repeat initial configuration script with downline and uplink disconnected from cassette
 - Same new error is seen which is confusing since there is nothing connected to the uplink so where is it reading data from? How is it receiving data words?
4. Re-flashed FEC12 Firmware
5. Went back to old setup
 - Same new error is seen which does not make sense since this was never seen in the old setup
6. Went back to new setup with cassette position 13 uplink and 1 on downlink (ran gpio test)
 - Ran cleanly (No timeout error seen and no new error)
7. Ran initial config test

- **Can successfully read ROMREG from the master IpGBT and returns expected value**

8. Power cycled and repeated step 7 to confirm outcome

- Result was repeatable

Results

We can confirm that we can now read and write to the master IpGBT. The new setup solved the previous issue of never receiving any data from the uplink. We no longer see timeout errors when the fanout fiber number 7 is connected to slot 1 and fiber number 6 is connected to slot 13 on the cassette.

In terms of the interesting new error that seemed random this issue was solved on July 22! It turns out BTL people had left a program running 24/7 on accident and it was attempting to send uhal commands to the FPGA, this was causing the errors since only one user can communicate with the FPGA on the Serenity at a time.

For more info as to why this happened see Alessio Boletti response:

"You are right, and indeed the goal is to have SPARC actually making any operation only when any of the trays is powered, to ensure its safety. In these days we were using a test version that had indeed the problem mentioned above, i.e. relying only on the presence on the lockfile, located in the /tmp of the serenity, to determine whether it had freedom to run commands. The way we were using this version was to manually delete the lockfile when we wanted to test operations, after taking the serenity, and recreating the lockfile before releasing it. The oversight was that upon reboot the lockfile would be deleted."